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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/707,448	11/07/2000	Jack D. Pippin	423901674C2D	8694

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.  
1940 DUKE STREET  
ALEXANDRIA, VA 22314

EXAMINER
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PROCTOR, JASON SCOTT

ART UNIT	PAPER NUMBER
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2123

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/22/2006	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

**Office Action Summary**

Application No.

09/707,448

Applicant(s)

PIPPIN, JACK D.

Examiner

Jason Proctor

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 October 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-11 and 13-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 and 13-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 November 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

Claims 3-11 and 13-21 were rejected in the Office Action of 26 May 2006.

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 28 August 2006 has been entered.

### ***Claim Interpretation***

Claim 7 does not appear to recite any limitation that defines the invention. Claim 7 merely recites additional functional language describing "the threshold adjustment logic." While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. Please see MPEP 2114.

It is further noted that claim 6 recites "threshold adjustment logic" and describes this feature in terms of functional language. As in claim 7, this functional language cannot be properly interpreted as defining the invention. The effective limitations of claim 6 are there "The integrated circuit of claim 5 further comprising threshold adjustment logic." Claim 7 effectively recites the same.

Claims 6 and 7 are neither rejected nor objected for the reasons stated above. The Examiner merely intends to draw Applicants' attention to a broad, reasonable interpretation of these claims to facilitate comparison to the prior art. Similar analysis is appropriate for the functional language of claims 3, 4, and 8-11.

### ***Response to Arguments – 35 USC § 103***

In response to the previous rejection under 35 U.S.C. § 103, Applicants argue primarily that:

Briefly recapitulating, claims 3 and 10 define an integrated circuit (IC) including a plurality of thermal sensors placed on the IC. Likewise, claims 14 and 20 define sensing temperature at a plurality of locations on an IC. As conceded in the official action, Kenny et al. merely teach a single thermal sensor and that the sensor is mounted near the circuit to be monitored. That is, the thermal sensor of Kenny et al. is not placed on the circuit to be monitored. By placing a plurality of sensors on the IC, the timing and accuracy of determining whether the IC is running hot is improved as compared to Kenny et al. which places the temperature sensor near the circuit being monitored.

Regarding the claim term "across the integrated circuit," the official action asserts that at broad reasonable interpretation of "across" means "into contact with." Applicant respectfully traverses. However, in order to expedite prosecution, without prejudice to pursue claims in the future reciting the claim term "across," Applicant has amended the independent claims to recite that the thermal sensors are placed on the integrated circuit. See by way of non-limiting example page 22, lines 14-21 of the specification. No further rejection of the basis of the combination of Kenny et al. and Emory et al. is therefore anticipated.

The Examiner responds as follows.

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Applicants' arguments have been fully considered and have been found persuasive. Neither the Kenny nor the Emery references expressly disclose placing a thermal sensor **on the circuit** to be monitored. The previous rejections under 35 U.S.C. § 103 have been withdrawn.

An updated search of the prior art has revealed a reference that expressly discloses placing a thermal sensor **on the circuit** to be monitored. Please see the new grounds of rejection below.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
  2. Ascertaining the differences between the prior art and the claims at issue.
  3. Resolving the level of ordinary skill in the pertinent art.
  4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
2. Claims 3-11 and 13-21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 5,287,292 to Kenny et al. in view of US Patent No. 4,602,872 to Emery et al., and further in view of US Patent No. 5,233,161 to Farwell et al. (hereafter referred to as Kenny, Emery, and Farwell respectively).

Regarding claims 3, 10, 13, 14, and 20, Kenny teaches an integrated circuit comprising a **single** thermal sensor to generate a temperature value,

a stored threshold value, and

interrupt logic and generating an interrupt if the temperature value exceeds the stored threshold value [*“the temperature of an integrated circuit is regulated using a conventional temperature monitor and a novel power user regulator”* (column 1, lines 51-64); regarding **thermal sensor**, *“a temperature dependent resistor 501 would be mounted near the circuit to be mounted”* (column 9, lines 38-52); regarding **interrupt logic** and **threshold value**, *“When the temperature as indicated by a signal on line 505 reached a trigger value the power use regulator 502 would activate”* (column 9, lines 38-52); regarding **generating an interrupt**, *“The power use regulator might simply force the integrated circuit to low clock speed operation as long as the temperature is high,”* (column 9, lines 38-52) where an internal computer signal to communicate with other peripheral devices, such as controlling clock speed, is an interrupt].

Kenny does not expressly suggest using a **plurality of thermal sensors** or an **averaging mechanism** as recited by the claim.

Emery teaches a temperature monitoring system for an electric generator, including specific teachings applicable to monitoring complex systems. In particular, Emery teaches a **plurality of thermal sensors** [*“a plurality of temperature sensors are positioned... to derive respective signals indicative of the temperature of [components of the electric generator]”* (column 2, lines 17-26)] and

**calculating an average temperature from the plurality of sensors** [*“the signals from all of the sensors are combined to derive an average”* (column 2, lines 17-26)].

Emery expressly provides motivation for averaging the values from a plurality of temperature sensors [*“a temperature sensor during a malfunction may provide an abnormally high reading from its previous normal reading, however such condition will go undetected [in the prior art]. The present invention provides for an improved temperature monitoring system for such generator wherein early detection of an abnormally hot stator coil is made possible”* (column 2, lines 2-14)]. In more detail, Emery teaches comparing each individual sensor reading against the average sensor reading, thereby determining “how far from average” each reading is rather than merely determining “how hot” each reading is, and thus producing a more reliable measure of heat in the device (column 2, lines 27-54)].

As with Kenny, Emery teaches a **threshold temperature** and generating an alarm if the threshold temperature is exceeded, directly analogous with generating an interrupt in a computer processor [*“Each of the generated percentage indications may be compared with first and second alarm limits to appropriately notify the operator should either of the alarm limits be exceeded”* (column 2, lines 50-53)].

Neither Kenny nor Emery explicitly teach **placing a temperature sensor on an integrated circuit** as recited by the claim.

Farwell teaches **placing a temperature sensor on an integrated circuit** [*“The burn-in heating circuit 10 includes a temperature sensing circuit 19 which is shown as being both on-chip and off-chip since it includes a temperature sensing component that must be on-chip, and*

*which is the only component of the burn-in heating circuit that must be on-chip.*" (column 2, lines 52-57); *"The heating circuit 10 further includes the temperature sensing circuit 19 which provides an output voltage CTEMP that is indicative of the junction temperature of the integrated circuit... By way of particular example, the temperature sensing circuit 19 can include an on-chip temperature sensing diode and a constant current source, which can be on-chip or off-chip, for providing constant current forward bias on the temperature sensing."* (column 3, lines 7-19)].

Farwell expressly provides motivation for placing a temperature sensor on an integrated circuit, such as precise on-chip temperature measurement [ *"Pursuant to the disclosed invention, precise on-chip temperature measurement is provided by temperature dependent devices, such as clamping diodes normally included in integrated circuit chips."* (column 5, lines 43-46)].

Kenny, Emery, and Farwell are all analogous art because all are drawn to the field of thermal measurement and control.

Therefore it would have been obvious to combine the teachings of Emery regarding averaging the readings from a plurality of thermal sensors to achieve a more reliable measure of heat in the device, and to combine the teachings of Farwell regarding placing a temperature sensor directly on an integrated circuit to obtain precise on-chip temperature measurement, with the integrated chip taught by Kenny including a clock speed controlled by thermal sensor. The incorporation of the Emery and Farwell teachings would both enhance the reliability and precision of the thermal control aspect of the Kenny invention.



Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Kenny, Emery, and Farwell to arrive at the invention specified in claims 3, 10, 13, 14, and 20.

In addition to the above, where claims 10 and 20 refer to **displaying information regarding the calculated average**, Emery expressly teaches generating alarms (column 2, lines 50-53) and alarm checks coupled to a display (FIG. 5B, references 112, 116, 108; *"Display apparatus 108 is provided in order to present... the results of the computation of percent of average coil temperature performed by circuit 102... If either of these [warning limits] are attained, such indication may be displayed such as by flashing the particular value or by a change in color, if the display apparatus includes a color monitor"* (column 8, lines 11-28)]. In forming the combination above, in light of the teachings of Emery regarding the display of alarms, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to include the display features taught by Emery in order to alert a user of the integrated circuit that a temperature threshold was surpassed, for example to prompt the user to adjust the usage of the integrated circuit and lower the measured temperature.

Where 14 and 20 define methods performed by the apparatuses of claims 3 and 10, these methods are performed by the combination formed above.

Regarding claims 4 and 15, Kenny expressly teaches adjustment logic to decrease a clock frequency in response to a signal indicating that the threshold temperature has been exceeded

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[*“The power use regulator might simply force the integrated circuit to low clock speed operation as long as the temperature is high,”* (column 9, lines 38-52)].

Regarding claim 5, wherein the **register is programmable by the integrated circuit**, Emery expressly teaches that the alarm limit values (*stored threshold values*) may be, “by way of example,” 3.0° C and 6.0° C (column 8, lines 46-49). Emery expressly suggests methods of calculating the alarm limits (column 8, lines 24-45). Emery clearly conveys to one of ordinary skill in the art that the alarm limit values (*stored threshold values*) should be adjusted to suit the needs of the application; that is, the means for storing or representing the alarm limit values (*register*) should be configurable or programmable. Thus, it would have been obvious to a person of ordinary skill in the art at the time of Applicants’ invention in the formation of the combination above in order to adjust the threshold values to suit the needs of a particular application.

Regarding claims 6-7, 11, 16-17, and 21, wherein **threshold adjustment logic** is used to **program the register to a different** (and **second different**) threshold temperature in response to an interrupt indicating that the threshold (and first threshold) temperature has been exceeded, these limitations construct a system where two signals are generated as the temperature exceeds a first and subsequently a second threshold, which is expressly taught by Emery [*“an alarm check circuit 112 is provided and is operable to compare each value provided by circuit 102 with a first or warning alarm limit, as well as with a second or shut down alarm limit”* (column 8, lines 11-28)]. The distinction between reprogramming a single threshold versus predetermining two

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distinct thresholds is considered an equivalent solution that would have been obvious to a person of ordinary skill in the art. In forming the combination above, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to incorporate the concepts of Emery regarding the use of two thresholds in order to create a graduated thermal control system, such as one with a "warning" stage and a more critical "shutdown" stage (see Emery, column 8, lines 30-45).

Regarding claims 8 and 18, wherein the clock adjustment logic is used to **control the temperature of the integrated circuit by increasing and decreasing an integrated clock frequency**, this limitation is expressly taught by Kenny [*"The power use regulator might simply force the integrated circuit to low clock speed operation as long as the temperature is high... The circuits would operate as long as the temperature monitor indicated high temperature, but would deactivate and reset [restoring high clock speed] when the temperature fell to an acceptable level"* (column 9, lines 38-52)].

Regarding claims 9 and 19, Emery teaches a "shutdown" threshold (column 8, lines 30-45) which would convey to a person of ordinary skill in the art a teaching that there exists some temperature threshold which, when exceeded, should indicate that the system being monitored should be halted. Further, Official Notice is taken that halting a computer component to conserve power or dissipate heat is old and well-known in the art (See US Patents 4,851,987 to Day; 4,204,249 to Dye et al.; 5,025,387 to Frane; 4,823,292 to Hillion; 5,189,647 to Suzuki et al.; among others). Therefore it would have been obvious to a person of ordinary skill in the art

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at the time of Applicants' invention to combine the teachings of Kenny and Emery, as cited above, and to incorporate the old and well-known method of halting a computer processor or component in order to conserve power or dissipate heat.

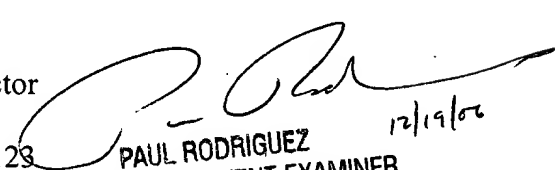
***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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